User's Guide

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For Safety and Regulatory information,
see the pages behind the index.

Agilent Technologies E5904B Option 500 FPGA Trace Port Analyzer

FPGA Trace Port Analyzer—At a Glance

Performing traditional in-circuit debug of systems that contain leading-edge FPGA designs can be difficult. To capture trace, internal nodes must be routed to FPGA pins. Routing critical internal FPGA nodes to external FPGA pins is costly in terms of pin count and PC board design. Deep trace memory may be necessary to capture enough event history to solve elusive problems.

Agilent and Xilinx deliver a high-value solution that couples the advantages of an internal logic analyzer with fast and deep external trace storage. This solution gives you debug insight into digital systems that contain Xilinx Virtex II and Virtex II Pro FPGAs while conserving pin count and providing deep memory.

The Agilent/Xilinx solution combines powerful capabilities:

- Agilent FPGA Trace Port Analyzer
- Agilent Trace Core
- Xilinx ChipScope Pro

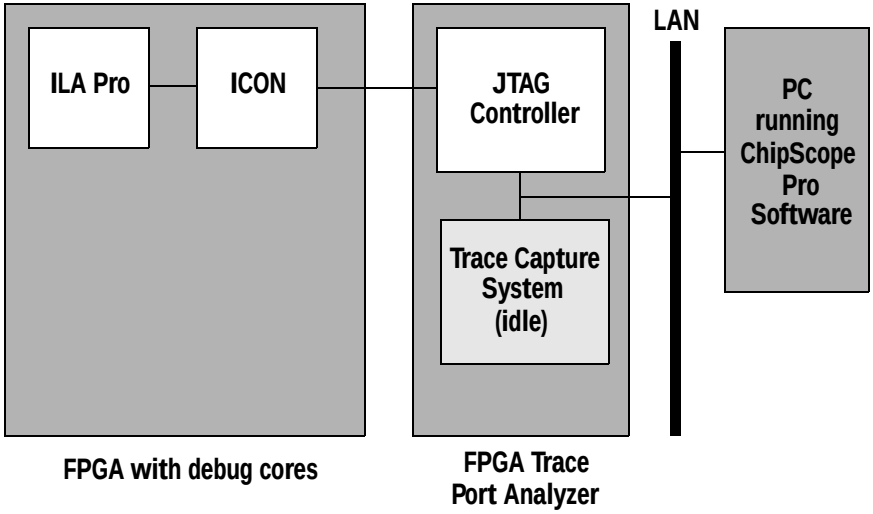
Using this solution, you can:

- Trigger on events internal to the FPGA
- Collect deep traces of internal FPGA activity while preserving all internal FPGA memory for other design purposes
- Efficiently debug using a fraction of the pins normally dedicated to debug

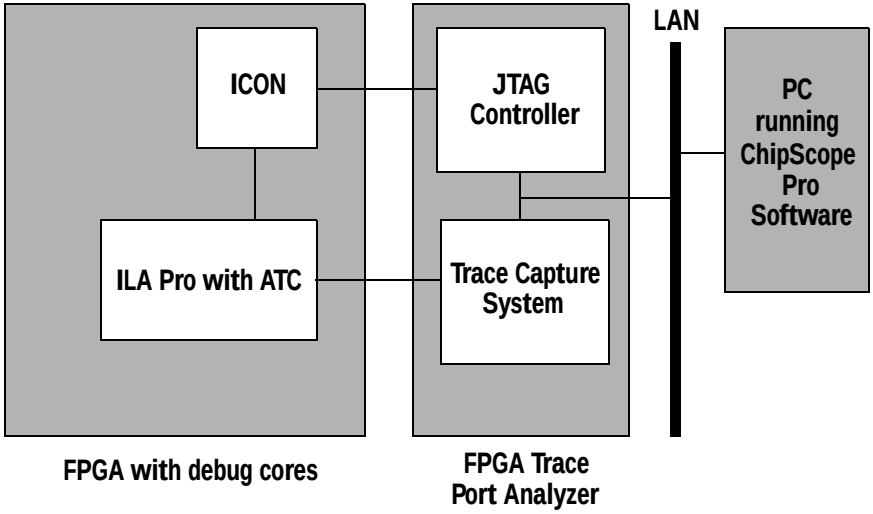
On-Chip Debug Cores

The Agilent E5904B Option 500 FPGA Trace Port Analyzer communicates with debug cores internal to the FPGA. The FPGA Trace Port Analyzer can be used with debug cores in three different use models:

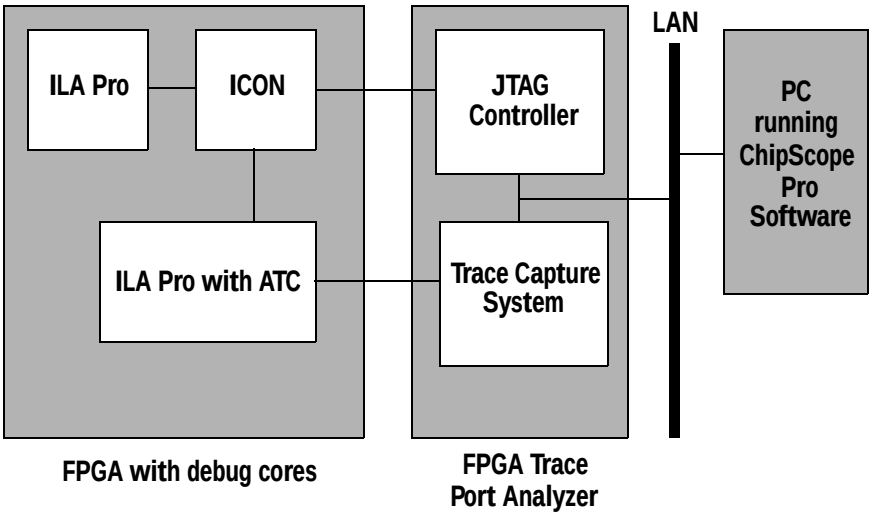
1. Xilinx Integrated Control (ICON) and Integrated Logic Analyzer (ILA) Pro when internal FPGA block RAM is used for trace memory.



2. Xilinx ICON with ILA Pro and Agilent Trace Core (ATC) when Agilent's FPGA Trace Port Analyzer is used for trace memory.



3. The preceding two methods used in tandem.



Xilinx ChipScope Pro provides the user interface to the ILA Pro with ATC. It configures the on-chip debug cores using a JTAG controller. ChipScope Pro also displays trace captured by the FPGA Trace Port Analyzer.

FPGA Trace Port Analyzer Overview

The Agilent Technologies E5904B Option 500 FPGA Trace Port Analyzer contains:

- A JTAG controller
- Trace capture system
- A LAN interface

JTAG Controller

Facilitates communication between ChipScope Pro and on-chip debug cores via JTAG. Among other tasks, the JTAG controller downloads trigger setup to ILA Pro, passes captured trace data to ChipScope Pro, and can be used for downloading FPGA configurations.

Trace Capture System

This subsystem collects output from the ILA Pro with ATC trace port.

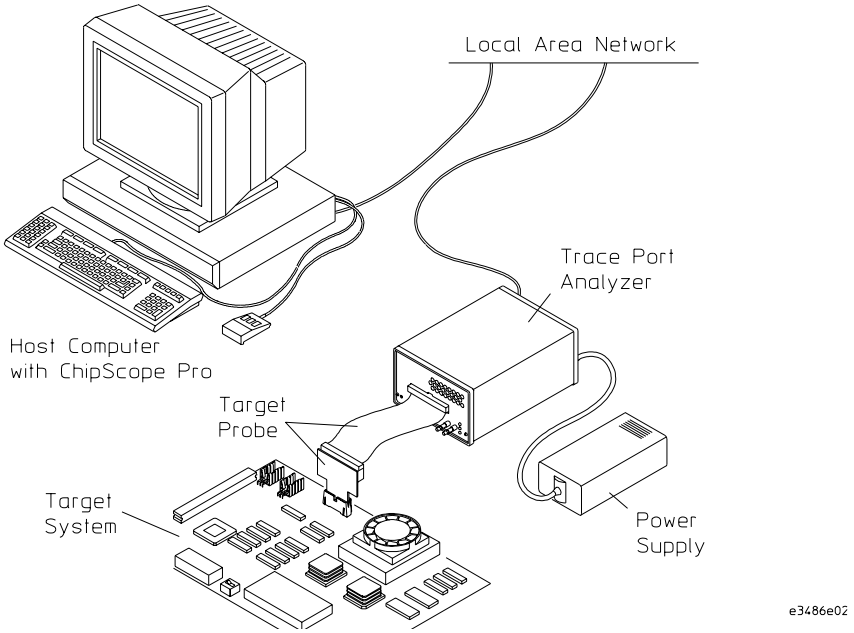
- Captures data on 4-, 8-, 12-, 16-, or 20-bit wide trace ports.
- Stores up to 2M trace states (1M trace states with up to 79 internal signals in 4X mode of the ATC)
- Captures data on ILA with ATC ports whose voltages are 1.8 V to 3.3 V.
- Sends a trigger signal to other instruments, or use signals received from other test instruments to trigger the FPGA Trace Port Analyzer.

The LAN Interface

The LAN interface provides communication between the FPGA Trace Port Analyzer and Xilinx ChipScope Pro software.

With the IEEE 802.3 Type 10/100Base-TX LAN connection, you can:

- Connect the FPGA Trace Port Analyzer to a target system in the lab and use Xilinx ChipScope software anywhere else on the LAN.
- Connect to either 10 Mbps (10BASE-T) or 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The FPGA Trace Port Analyzer automatically negotiates the data rate for the LAN it is connected to.)



ChipScope Pro Software

The FPGA Trace Port Analyzer must be used with Xilinx ChipScope Pro software, version 5.1i or greater.

The Xilinx ChipScope software will let you:

- Download FPGA configurations.
- Set triggers, trigger sequences, etc., in the ILA Pro cell using the JTAG controller unit of the FPGA Trace Port Analyzer.
- Import captured trace information from the FPGA Trace Port Analyzer to the ChipScope Pro viewer.

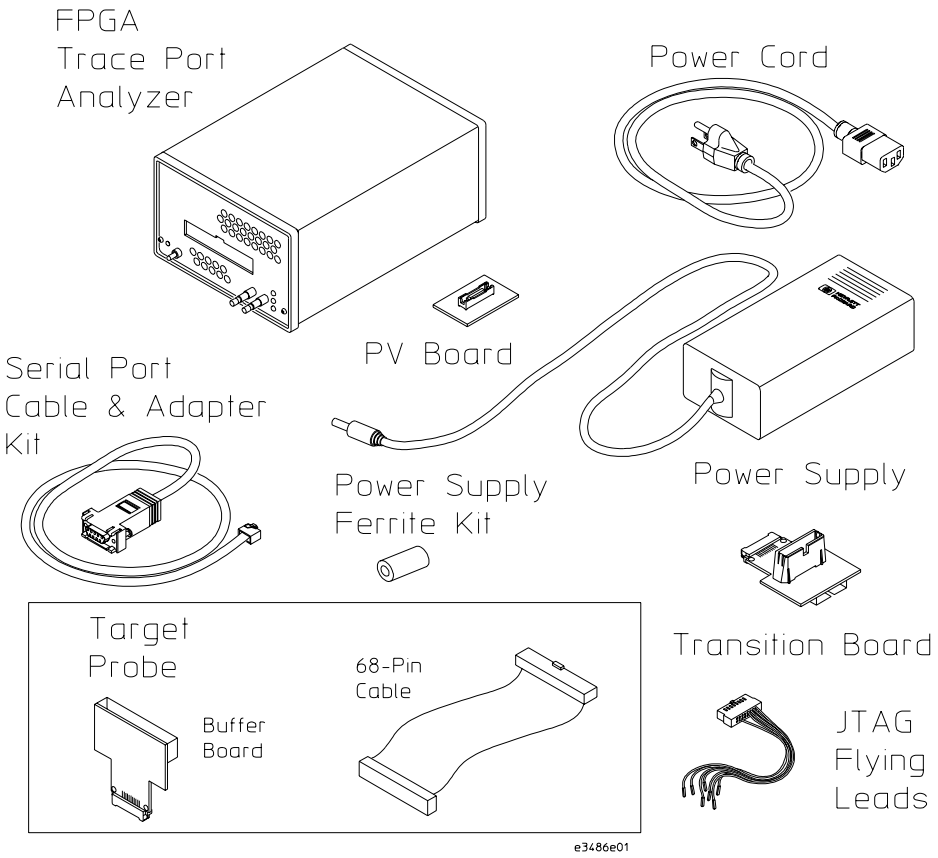
FPGA Families Supported

The Agilent Technologies E5904B Option 500 FPGA Trace Port Analyzer supports the following FPGAs when they include the ILA with ATC.

FPGAs Supported
Xilinx Virtex II
Xilinx Virtex II Pro

Equipment Supplied

The Agilent Technologies E5904B Option 500 FPGA Trace Port Analyzer consists of:



Part number	Description
E3486-60002	FPGA Trace Port Analyzer Unit
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Power supply ferrite kit
E3486-66503	Transition Board
E3499-61600	JTAG Flying Leads
E5903-61602	68-pin cable
E5903-66507	Buffer board
E5903-66509	PV board
E8130-68702	Serial cable and adapter
E3486-970xx	This user's guide

In This Book

This book is the user's guide for the Agilent Technologies E5904B Option 500 FPGA Trace Port Analyzer. It describes:

- Target system design considerations and other requirements of the FPGA Trace Port Analyzer.
- How to connect the FPGA Trace Port Analyzer to a LAN, configure it, and connect it to the target system.
- How to coordinate measurements between the FPGA Trace Port Analyzer and other test instruments.
- How to update FPGA Trace Port Analyzer firmware.
- How to troubleshoot and solve problems.
- Characteristics of the FPGA Trace Port Analyzer.

See Also

See the user's guide manual for Xilinx ChipScope Pro for more information.

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Target System Design Considerations

To use the Agilent Technologies E5904B Option 500 FPGA trace port analyzer, the FPGA must have the ILA with ATC, and the trace port signals should be routed to a header connector on the target system.

When integrating the ILA with ATC into an FPGA, the quality and timing of the trace port signals to the FPGA trace port analyzer are critical for reliable operation. Some of the FPGA and printed-circuit board design issues to consider are:

- Output pad selection.
- Printed-circuit board track lengths.
- Printed-circuit board track termination.
- Setup and hold times for the trace data signals with respect to ATCLK.

The care that must be taken with the design of the trace port is generally proportional to the frequency of operation. At frequencies of more than 100 MHz careful SPICE analysis of the system, including the characteristics of the package should be taken into account.

Early attention to the design guidelines can ensure correct operation of the FPGA trace port analyzer.

This chapter describes:

- Printed-circuit board design guidelines.
- The target system header connector and required signals.
- Height restrictions and keep-out requirements.
- Timing and voltage specifications for trace port signals.
- Transition board for use with non-standard header connectors.

Trace Port Signal Overview

The trace port signals consist of all of the signals provided by the ILA with ATC and the JTAG signals. These two groups of signals are combined onto a single connector to save space on the target system.

The trace port signals are described below.

Signals for Trace Port Analysis

ATCLK. The trace clock signal provides the clock for the trace port. ATD [n-1:0] signals are referenced to the rising edge of the trace clock with a single data rate trace port.

ATD[n-1:0]. The trace data signals are used to output internal trace states from the ILA. The data signals can be designed as 4-, 8-, 12-, 16-, or 20-bits wide.

Signals for both Trace Port Analysis and JTAG Control

Vref. The Vref signal is intended to supply a logic-level reference voltage to allow the FPGA trace port to adapt to the signal levels of the target board.

Outputs to target systems are clamped at Vref on high level outputs. Inputs from the target system are sensed in reference to the Vref voltage level.

NOTE: Vref does NOT supply operating current to the debug equipment.

Target board should supply a Vref voltage that is between 1.65 V and 3.6 V. The target board should provide a sufficiently low DC output impedance so that the output voltage will not change by more than 1% when supplying a nominal signal current (± 0.4 mA).

Signals for JTAG Control

TDI. TDI is the Test Data In signal from the JTAG unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TMS. TMS is the Test Mode Select signal from the JTAG unit to the target JTAG port. This pin must be pulled up on the target so that the effect of any spurious TCKs when there is no connection is benign.

TCK. TCK is the Test Clock signal from the JTAG unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TDO. TDO is the Test Data Out from the target JTAG port to the JTAG unit.

FPGA Design Guidelines

FPGA Pad Selection and Placement

The position and type of pad selected is based on the following factors:

- Minimizing noise and coupling between trace and other signals.
- Ability to drive the external load.

It has been shown that the quality of the ATCLK signal, as observed by the FPGA trace port analyzer, has the greatest effect on the reliability of the system. The ATCLK transition *must* move cleanly through the threshold region of the input circuitry of the FPGA trace port analyzer, without glitches or ringing.

With certain types of package and pin placement, the signal coupling between the trace data signals and the trace clock can be significant. If this is observed to be a problem during simulations, it is recommended that GND or static I/O signals are placed on both sides of the ATCLK signal.

Contact Xilinx for other high-speed FPGA design considerations.

Printed-Circuit Board Design Guidelines

The FPGA trace port analyzer should be the only load on the nodes connected to the FPGA's trace port pins. The main concern is signal integrity at the FPGA trace port analyzer connector.

The JTAG signals from the FPGA Trace Port Analyzer connector should be routed according to Xilinx recommendations.

The slower JTAG signals allow reduced PC board design constraints, but the JTAG TCLK signal needs to have good monotonic signal quality.

Printed-Circuit Board Track Length

Match all ATCLK, and ATD[n-1:0] track lengths between the FPGA and the trace port connector within 100 ps. Overall differences of greater than 100 ps in track lengths directly impact setup and hold requirements. If the clock is delayed compared to the data, the setup specification needs to be increased by the additional clock delay. If any data is delayed compared to the clock, the additional delay needs to be added to the setup requirement. If data paths are such that data has both greater than and less than delays compared with the clock, the difference needs to be added to both the setup and hold specification.

Signal Quality

Reflections, overshoot, and undershoot all need to be minimized to ensure accurate data acquisition. The primary variable is the rise time of a signal compared to its track length. This is where the minimum signal rise and fall time becomes important.

The following points should be considered:

1. Ensure the one way propagation time for all tracks is less than 1/3 of signal rise time.
2. If tracks must be longer than 1/3 of the signal rise time, then some form of signal termination is required. The recommended method is series termination or using Xilinx DCI outputs. The series resistor must be placed as close as possible to the FPGA pin. The value of this series resistor, when added to the output impedance of the signal driver should closely match

the impedance of the printed-circuit board track.

3. If the total track length is one rise time propagation delay or longer in length, follow standard high-speed design practices to minimize cross talk between the clock and the data signals.

Be aware that as the fabrication process for your FPGA improves, your output driver will probably improve and your rise and fall times decrease. If you are close to violating the requirements of point 1, consider adding termination to the signals to ensure continued correct operation.

Header Connector Requirements

The target header is an AMP MICTOR Connector (0.64mm [0.025in]) pitch. The header has 38 pins and is organized such that it can handle:

- up to 20 trace data pins
- 1 trace clock pin
- 1 voltage reference pin
- 4 JTAG pins

Recommended Orientation

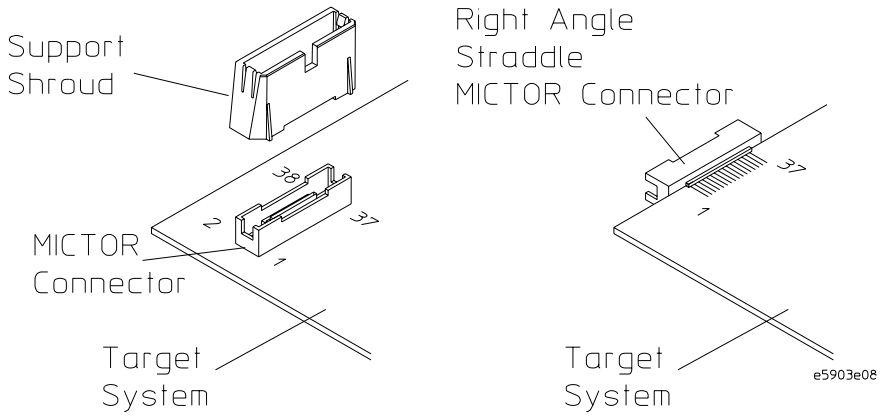
There are two choices for the target header: a vertical connector, and a right angle straddle mount connector.

The vertical connector is recommended because it can accommodate an optional support shroud that provides additional strain relief and thus greater reliability. The notch on the support shroud should be placed on the same side as the odd numbered pins on the MICTOR connector. The support shroud is highly recommended.

The straddle mount connector should be used when board real estate is at a premium and there is no room for the vertical connector. A support shroud is not available for use with the straddle mount connector.

The recommended ILA with ATC trace port connector orientation is displayed in the following diagram.

Connector Orientation



Connector and Support Shroud Part Numbers

The AMP part numbers for the MICTOR target headers are given below. These connectors may be purchased directly from AMP. Support shrouds and kits of five MICTOR connectors and support shrouds may be purchased from Agilent.

AMP MICTOR Headers Available from AMP

AMP Part Number	Description
2-767004-2	Vertical surface mount connector Ground bus lead length 1.397 mm (0.055”)
767054-1	Vertical surface mount connector Ground bus lead length 2.743 mm (0.108”)
767061-1	Vertical surface mount connector Ground bus lead length 3.505 mm (0.138”)
767044-1	Horizontal straddle mount connector

Support Shrouds Available from Agilent

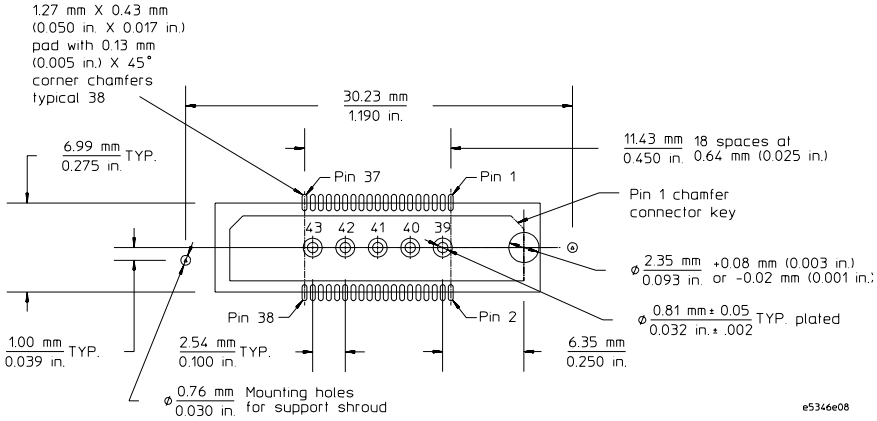
Agilent Part Number	Description
E5346-44701	Vertical support shroud for PCB thickness up to 1.575 mm (0.062”)
E5346-44704	Vertical support shroud for PCB thickness from 1.575 mm (0.062”) to 3.175 mm (0.125”)
E5346-44703	Vertical support shroud for PCB thickness from 3.175 mm (0.125”) to 17.780 mm (0.70”)

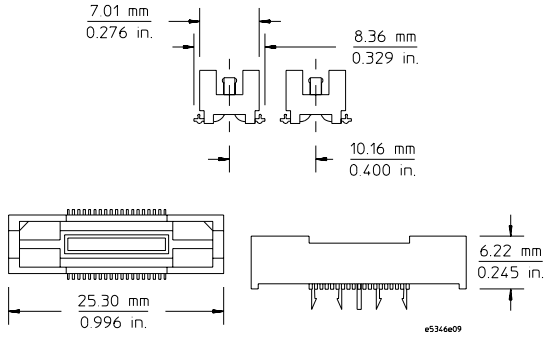
Set of Five MICTOR Connectors and Five Support Shrouds Available from Agilent

Agilent Part Number	Description
E5346-68701	Set of 5 MICTOR connectors and shrouds For PCB thickness up to 1.575 mm (0.062”)
E5346-68700	Set of 5 MICTOR connectors and shrouds For PCB thickness from 1.575 mm (0.062”) to 3.175 mm (0.125”)

Connector Dimensions

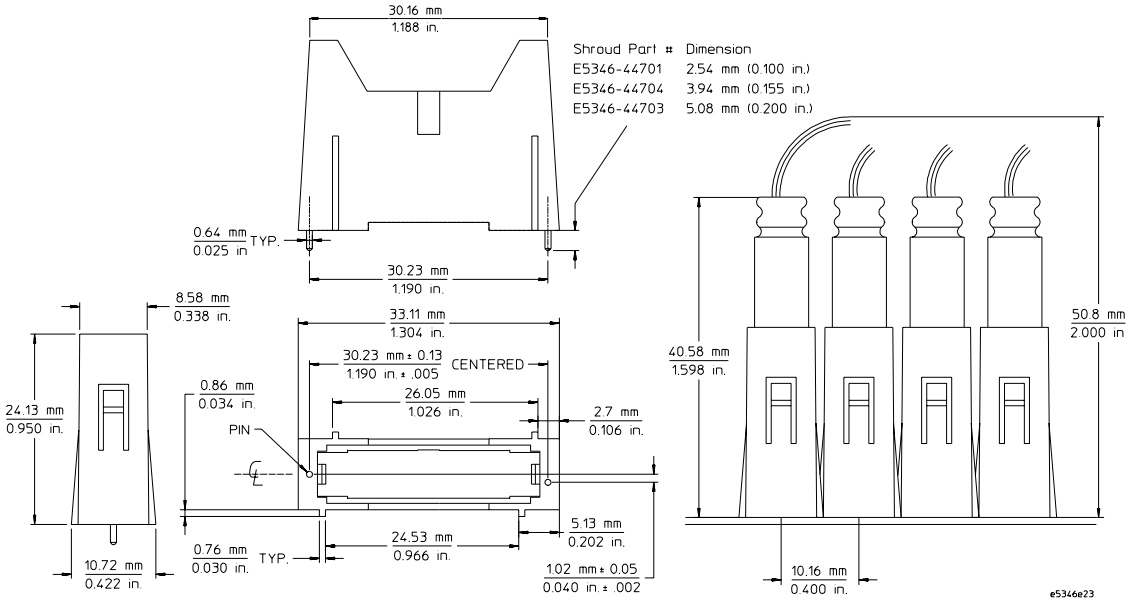
AMP MICTOR Connector Dimensions (AMP part # 2-767004-2)





Support Shroud Dimensions

Support Shroud Dimensions



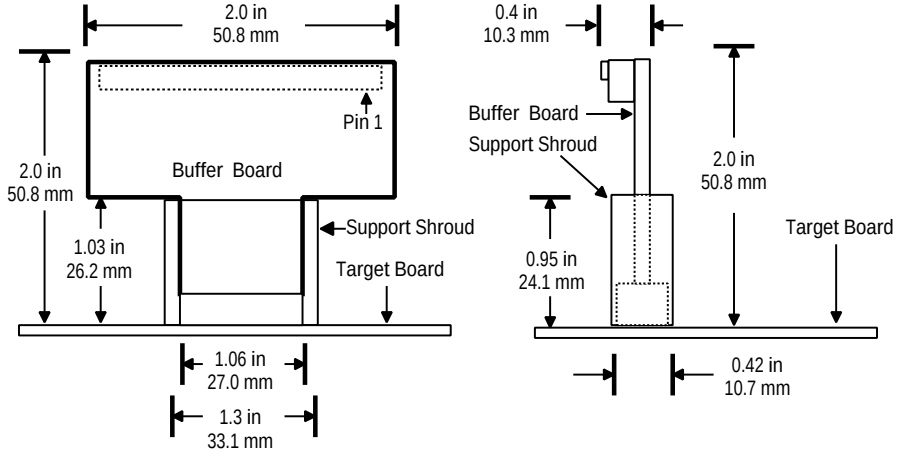
Height Restrictions and Keep-Out Requirements

The Agilent Technologies E5904B Option 500 FPGA trace port analyzer connects to the target MICTOR header with a small target probe (which is the 68-pin cable and a buffer board). The target probe connects either vertically or horizontally (right-angle), depending on which MICTOR header is on the target system.

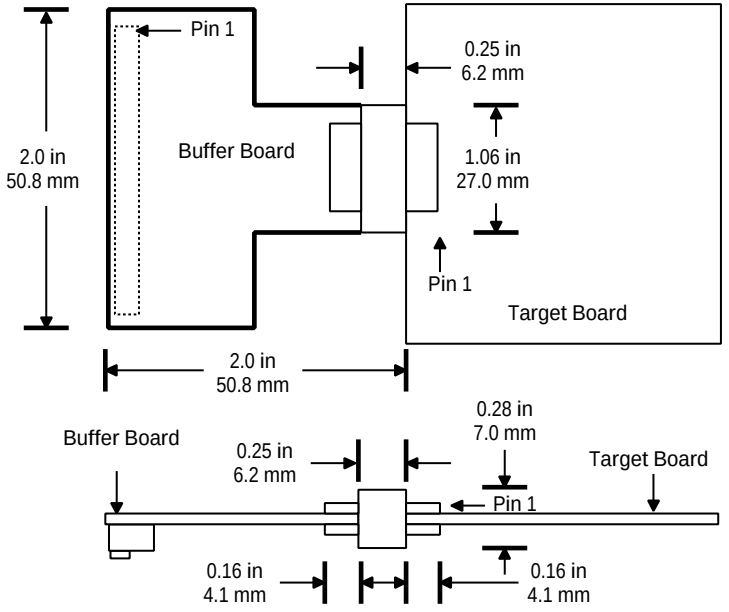
If the vertical header is used, make sure there is sufficient height clearance between the target system and the interface boards.

This section describes the height restrictions and keep-out for target header connectors using the buffer board (Agilent part number E5903-66507).

Buffer Board (E5903-66507), Vertical Header, and Support Shroud



Buffer Board (E5903-66507) and Right Angle Connector



Target Header Connector Pin-Out

The FPGA trace port analyzer connects to a MICTOR connector on the target system through the supplied buffer board, as shown on page 67.

The target header may also be used to connect other equipment to the target system, such as:

- PowerPC 405 debug trace (for Virtex II Pro devices with PowerPC core)
- A logic analyzer

The following diagram shows the MICTOR connector pinout for the header on the target system.

Target Header Pin-Out for the MICTOR Connector

No Connect*	1	2	No Connect*
No Connect*	3	4	No Connect*
No Connect	5	6	ATCLK
No Connect*	7	8	No Connect*
No Connect*	9	10	No Connect*
TDO	11	12	Vref
No Connect*	13	14	No Connect
TCK	15	16	ATD19
TMS	17	18	ATD18
TDI	19	20	ATD17
No Connect*	21	22	ATD16
ATD15	23	24	ATD7
ATD14	25	26	ATD6
ATD13	27	28	ATD5
ATD12	29	30	ATD4
ATD11	31	32	ATD3
ATD10	33	34	ATD2
ATD9	35	36	ATD1
ATD8	37	38	ATD0

NOTE:

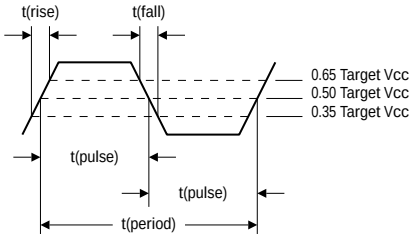
* Pins 1, 2, 3, 4, 7-10, 13, and 21 *must* be true no-connects. Pins 1-4 are driven when a logic analyzer is connected to the target system through the header connector. Pins 7-10, 13, and 21 are driven by the trace port analyzer.

For designs with less than 20 trace data pins, any unused ATD pins *must* be connected to ground.

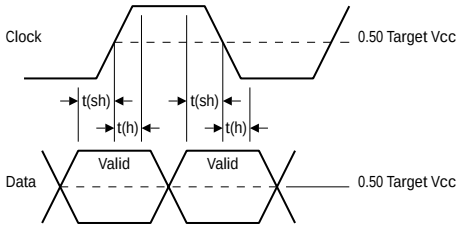
Timing and Voltage Specifications for Trace Port Signals

The signals from the target system must meet certain timing and voltage requirements in order for the Agilent Technologies E5904B Option 500 FPGA trace port analyzer to work correctly.

Signal Requirements



Clock Timing



Data Timing

Signal Requirements	
Maximum state clock frequency, single edge (single clock mode) t(period) = 1/frequency	200 MHz (1.65 Volts to 3.6 Volts Target Vref) 5 ns
Minimum clock pulse width, t(pulse)	2 ns (see note 1)
Maximum clock/data rise and fall time, t(rise) and t(fall)	3.6 ns (see note 1)
Minimum clock/data rise and fall time	See PCB guidelines
Data setup/hold times, t(su)/t(h)	1.5/1.0 ns (see notes 2 and 3)

NOTES:
1. Clock/data rise and fall times are measured between 35% and 65% of Target Vref or ± 30% of programmed threshold.
2. Setup/hold is measured at Target Vref/2 or at programmed threshold.

Buffer Board—Required Voltage Levels

Absolute Maximum Ratings	Minimum	Maximum
Target Vref	-0.5 V	4.6 V [1]
Clock and Data	-0.5 V	4.6 V [1]
Input Current (Input < -0.05 V)		-50 mA

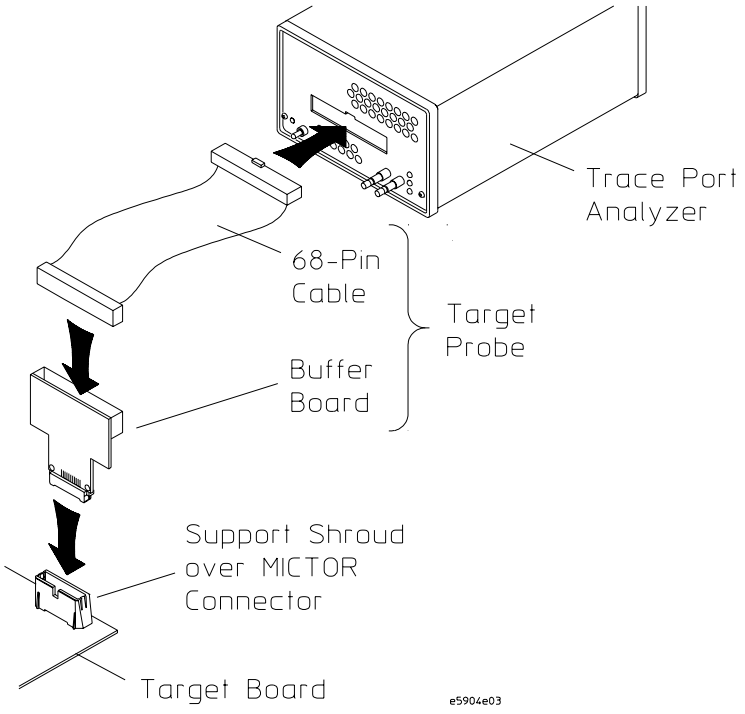
[1] Minimum voltage can be exceeded if maximum current rating is observed.

Recommended Operating Range	Minimum	Maximum
Target Vref	1.65 V	3.6 V
Clock and Data	0.0 V	3.6 V

DC Electrical Characteristics	Minimum	Maximum
Target Vref range	1.65 V	3.6 V
V_{ih}	0.65 Vref	
V_{il}		0.35 Vref

Loading Effects

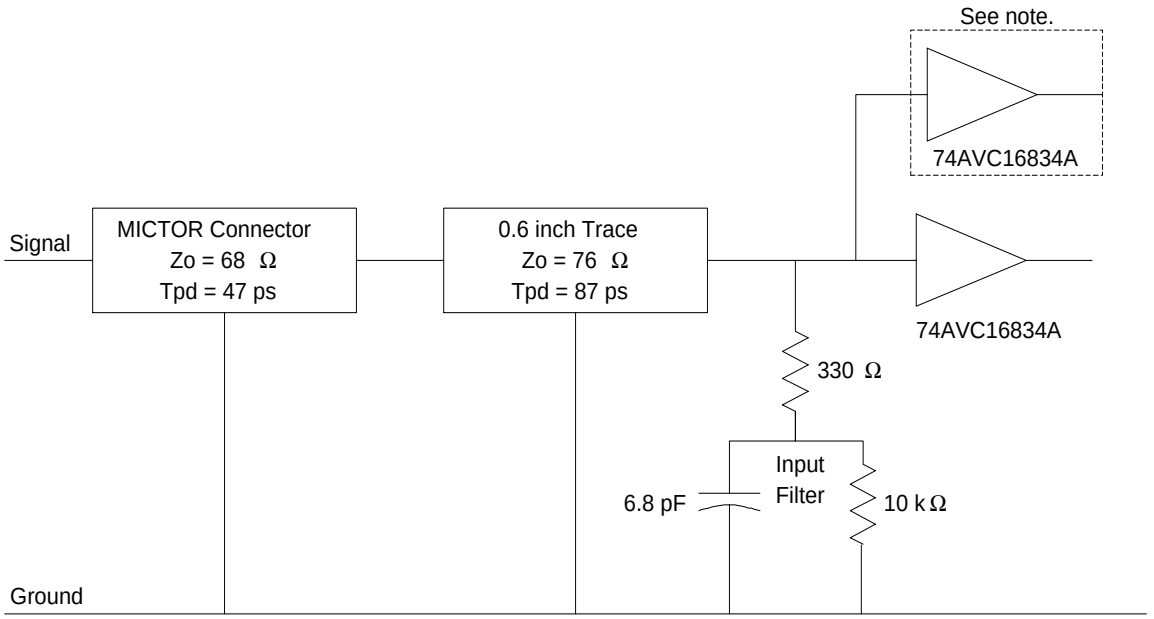
The FPGA trace port analyzer connects to the target system via the target probe as shown below:



Target Probe Equivalent Load

The FPGA trace port analyzer presents the following equivalent load to each signal. Target systems must be capable of driving this load and meeting the signal requirements given on page 31.

FPGA Trace Port Analyzer Buffer—Equivalent Load Model



NOTE: ATCLK drives an additional gate on the E5903-66507 buffer board. All other signals drive only one gate.

FPGA trace port analyzer probe characteristics (including buffer board)	
Input resistance (DC)	10 kΩ ± 5%
Input capacitance, data inputs	4.0 pF
Input capacitance, clock input	6.5 pF
Maximum input voltage (all inputs)	3.6 Volts

Modeling the Trace Port Analyzer Buffer Board

The following characteristics can be used to model the FPGA trace port analyzer buffer board.

MICTOR Connector

The MICTOR connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 Ω and Tpd = 47 ps.

PC Board

- The FPGA trace port analyzer buffer board has the following characteristics:
  - trace width = 0.127 mm (0.005 inches)
  - trace thickness = 0.0178 mm (0.0007 inches)
  - microstrip trace for ATCLK and ATD[n-1:0] signals
  - distance from traces to ground plane = 0.178 mm (0.007 inches)
  - spacing between traces = 0.508 mm (0.020 inches)
  - ground plane thickness = 0.0356 mm (0.0014 inches)
  - trace length = 15.24 mm (0.6 inches)
  - Er = 4.8

or

  - Zo = 76 Ω, Tpd = 87 ps

Input Filter

In place of the buffer board characteristics, you can use discrete models of 330 Ω, 6.8 pF, and 10 kΩ as shown in the figure on page 34.

Buffer IC

Use the IBIS model of a Philips 74AVC16834A IC in a TSSOP package. This model can be found on the Philips Semiconductor web site at:

http://www.philipslogic.com/support/ibis/avc/

The ATCLK signal is connected to two inputs of the buffer IC on the E5903-66507. Data signals are only connected to one input of the buffer IC.

Undershoot/Overshoot

Undershoot must not go below -0.5 V at the input of the buffer IC. Overshoot must not go above 4.6 V at the input of the buffer IC.

Trace Only Header Connector

For target systems that do not comply with the connector pinout shown on page 29 (which includes both JTAG and trace signals), a transition board and JTAG flying lead set are provided. The transition board and flying lead set allow the JTAG signals from the trace port analyzer to be connected to the target system via an alternate connector, such as the 2 mm pitch square pin connector that is used on many existing JTAG cables. The MICTOR connector pinout is shown below. See page 68 for connection details.

Target Header Pin-Out for the MICTOR Connector—Trace Only

No Connect*	1	2	No Connect*
No Connect*	3	4	No Connect*
No Connect	5	6	ATCLK
No Connect	7	8	No Connect
No Connect	9	10	No Connect
No Connect	11	12	No Connect
No Connect	13	14	No Connect
No Connect	15	16	ATD19
No Connect	17	18	ATD18
No Connect	19	20	ATD17
No Connect	21	22	ATD16
ATD15	23	24	ATD7
ATD14	25	26	ATD6
ATD13	27	28	ATD5
ATD12	29	30	ATD4
ATD11	31	32	ATD3
ATD10	33	34	ATD2
ATD9	35	36	ATD1
ATD8	37	38	ATD0

NOTE: * Pins 1, 2, 3, and 4 *must* be true no-connects. Pins 1-4 are driven when a logic analyzer is connected to the target system through the header connector. For designs with less than 20 trace data pins, any unused ATD pins *must* be connected to ground.

See Also See "Using a Non-Standard Header Connector" on page 68 for more information.

Transition Board

Using the transition board will degrade signal integrity. The transition board should only be used if the target system was not designed with the connector described on page 29.

The following characteristics can be used to model the FPGA trace port analyzer transition board.

MICTOR Connector

The MICTOR connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 Ω and Tpd = 47 ps.

PC Board

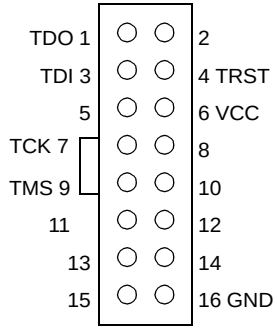
Zo = 100 Ω, Tpd = 1.67 ns

JTAG Flying Lead Set Pinout

Wire Colors

Signal	Pin	Wire Color
TDO	1	Blue
TDI	3	White
TCK	7	Green
TMS	9	Orange
TRST	4	Yellow
VCC	6	Red
GND	16	Black

Connector Pin-Out



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Connecting to a Power Source

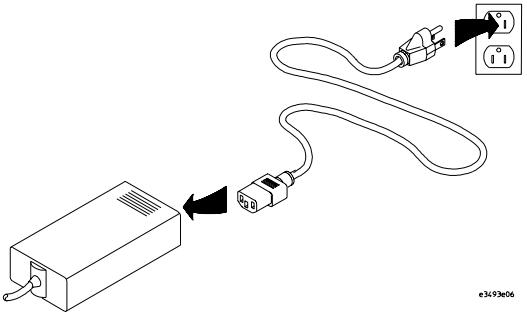
To connect the power supply

The FPGA trace port analyzer is shipped from the factory with a power supply and cord appropriate for your country. (The power supply you received may look different from the illustration below.) If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office (see "Contacting Agilent Technologies" on page 102).

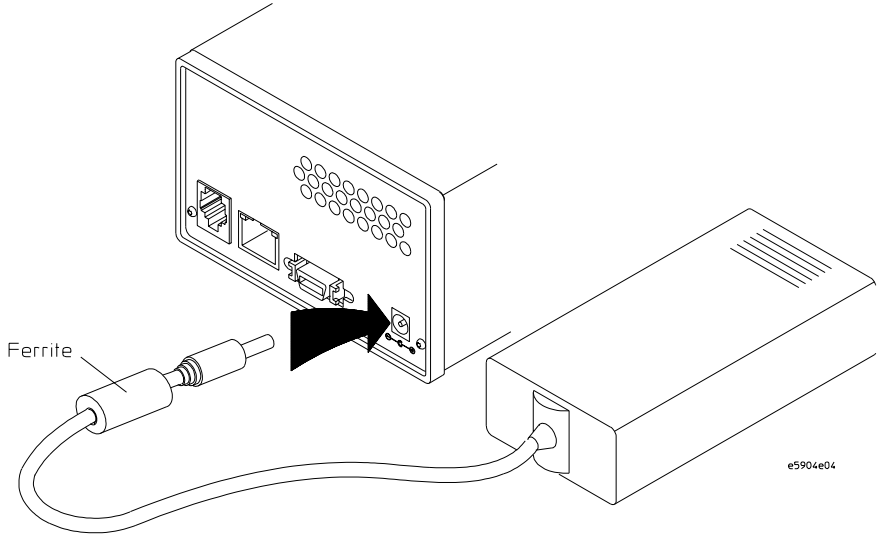
WARNING: **Use only the supplied Agilent Technologies power supply and cord. Failure to use the proper power supply could result in electric shock.**

CAUTION: Use only the supplied Agilent power supply and cord. Failure to use the proper power supply could result in equipment damage.

1. Install the ferrite on the 12 V power cord, near the end that plugs into the FPGA trace port analyzer.
2. Connect the power cord to the power supply and to a socket outlet.



3 Connect the 12 V power cord to the back of the FPGA trace port analyzer.

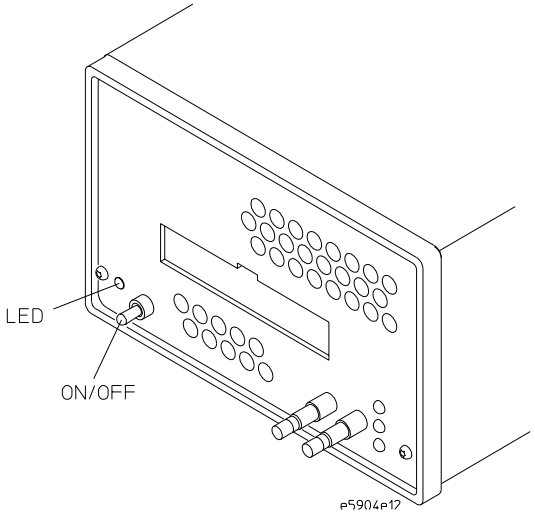


Ensure the power supply plug is completely seated in the power input receptacle.

To turn power ON

This procedure is for the FPGA trace port analyzer before it has been connected to a target system. (For the power ON procedure when connecting to a target system, see Chapter 5, “Connecting to a Target System,” on page 63.)

1 Turn ON the FPGA trace port analyzer power switch.



To turn power OFF

This procedure is for the FPGA trace port analyzer before it has been connected to a target system. (For the power OFF procedure when connected to a target system, see Chapter 5, “Connecting to a Target System,” on page 63.)

1 Turn OFF the FPGA trace port analyzer power switch.

3

Connecting to a LAN

Before the Xilinx ChipScope software can communicate with the FPGA trace port analyzer, the FPGA trace port analyzer must be connected to the LAN and set up with the proper LAN parameters.

The FPGA trace port analyzer has an IEEE 802.3 Type 10/100Base-TX LAN connector and is compatible with both 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The FPGA trace port analyzer automatically negotiates the data rate for the LAN it is connected to.)

NOTE:

If the FPGA trace port analyzer is already active on the LAN and you wish to change its LAN parameters, you can use a "telnet" command on a networked computer to connect to the FPGA trace port analyzer; then, use the built-in "lan" command to change LAN parameters.

After making LAN parameter changes, you must cycle power to the FPGA trace port analyzer before the changes take effect. Doing this will break the network connection and end the telnet session.

Step 1. Decide on the LAN setup method

The FPGA trace port analyzer can be set up on the LAN (in other words, its LAN parameters can be configured) in two ways:

- By a DHCP (Dynamic Host Configuration Protocol) server that responds to BOOTP requests.
- By using a computer with terminal emulation software (or by using an actual terminal) connected to the FPGA trace port analyzer's serial (RS-232) port, and by entering commands to set the LAN parameters.

What is DHCP?

DHCP (Dynamic Host Configuration Protocol) allows clients (like the FPGA trace port analyzer) to obtain LAN parameters automatically from a server.

How does the FPGA trace port analyzer use DHCP?

The FPGA trace port analyzer uses "static allocation" (sometimes called "manual allocation") to obtain a permanent IP address. Every time the FPGA trace port analyzer is turned on, it sends out a BOOTP request packet. If the DHCP server on the network responds to BOOTP requests and has been configured to reply to the FPGA trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

The FPGA trace port analyzer does not support "automatic allocation", which permanently allocates IP addresses from a pool of addresses.

Nor does the FPGA trace port analyzer support "dynamic allocation" of IP addresses—it does not track lease duration and request a new IP address when the lease is about to expire.

How does DHCP interact with other methods of setting LAN parameters?

Every time the FPGA trace port analyzer is turned ON, it sends out a BOOTP request packet (even if the LAN parameters have already been configured). As long as the DHCP server is configured to reply to BOOTP requests from the FPGA trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

Step 2. Set the FPGA trace port analyzer's LAN parameters

- Find out whether port numbers 6470 and 6471 are already in use on your network and if that use constitutes a conflict.

  Computers on the network which are running Xilinx ChipScope software can communicate with the FPGA trace port analyzer through two TCP service ports. The default base port number is 6470. The second port has the next higher number (default 6471).

  In almost all cases, the default numbers (6470, 6471) can be used without change. If necessary, the base port number LAN parameter can be changed (using a serial port connection) if the port numbers conflict with some other product on your network.

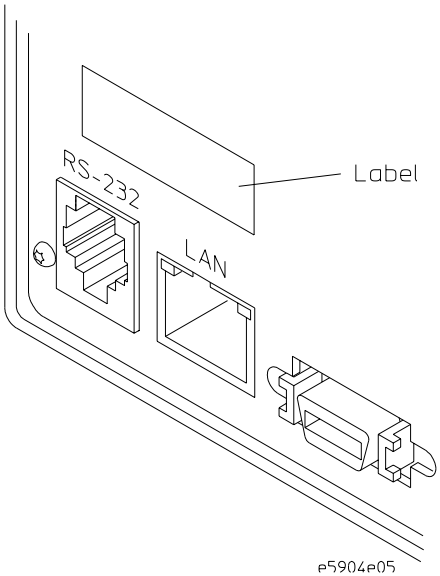
To set LAN parameters using DHCP

If there is a DHCP server on your network which responds to BOOTP requests and supports "static allocation" of IP addresses, it can be used to set the FPGA trace port analyzer's LAN parameters.

- Ask your system administrator to set up the IP address and other LAN parameters for the FPGA trace port analyzer on the DHCP server.

  You will need to supply the link-level address of the FPGA trace port analyzer.

  The link-level address (LLA) is printed on a label above the LAN connector on the FPGA trace port analyzer. This address is configured in each FPGA trace port analyzer shipped from the factory and cannot be changed.



To set LAN parameters using a serial port connection

The Agilent Technologies E5904B Option 500 FPGA trace port analyzer has a 9600 baud RS-232 serial interface with an RJ12 connector.

The FPGA trace port analyzer is shipped with a serial cable (with RJ-12 connectors on both ends, with 6-wire straight-through connections) and an adapter (female RJ-12 to female 9-pin D subminiature). The adapter plugs into 9-pin serial ports found on most PCs.

Serial connections on a workstation

If you are using a UNIX® workstation as the host computer, you need to use a serial device file. If a serial device file does not already exist on your host, you need to create one. Once it exists, you need to ensure that it has the appropriate permissions so that you can access it. See the system documentation for your workstation for help with setting up

a serial device.

Serial connections on a personal computer

Serial connections are supported on personal computers. (You must use hardware handshaking if you will use the serial connection for anything other than setting LAN parameters.)

If you are using a personal computer as the host computer, you do not need to set up any special files.

1 Get the following information from your local network administrator or system administrator:

- An IP address for the FPGA trace port analyzer.

  You can also use a "LAN name" or "hostname" for the FPGA trace port analyzer, but you must configure it using the integer dot notation (such as 127.0.0.1).

- The gateway address.

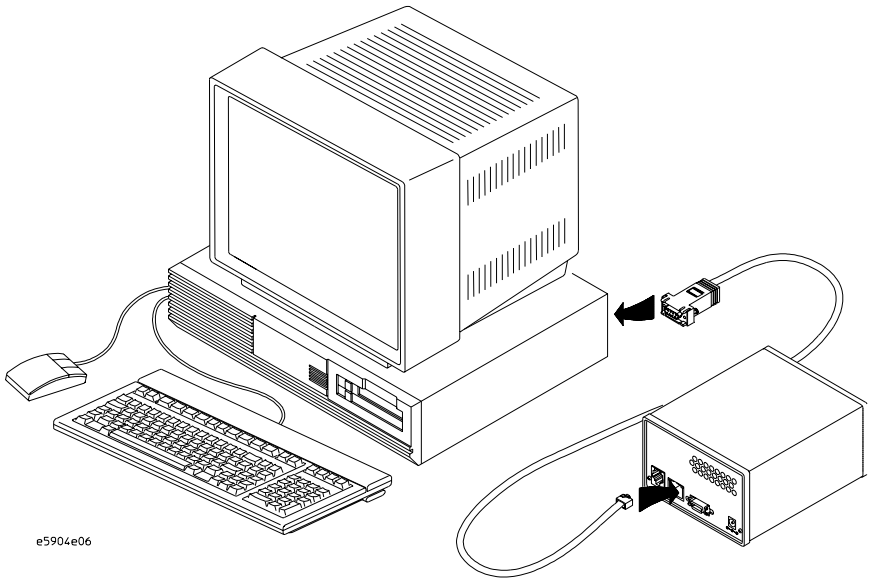
  The gateway address is an IP address and is entered in integer dot notation. The default gateway address is 0.0.0.0, which allows connections only on the local network or subnet. If connections are to be made to workstations on other networks or subnets, this address must be set to the address of the gateway machine.

- The subnet mask.

  A subnet mask blocks out part of an IP address so that the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.248.0.

2 Connect the serial cable from the host computer to the FPGA trace port analyzer.

Use the DB9-to-RJ12 adapter and the serial cable supplied with the FPGA trace port analyzer.



3 Start a terminal emulator program on the host computer.

If you are using a personal computer, the HyperTerminal application in Microsoft Windows® will work fine.

If you are using a UNIX workstation, you can use a terminal emulator such as cu or kermit.

4 Configure the terminal emulator program for:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

5 Turn on power to the FPGA trace port analyzer.

When the FPGA trace port analyzer powers up, it sends a version message to the serial port, followed by a prompt.

6 Press the Return or Enter key a few times.

You should see a prompt such as "p>" or "R>".

If you don't see a prompt, refer to "If there are serial port connection problems".

For information about the commands you can use, enter "?" or "help" at the prompt.

7 Display the current LAN parameter settings by entering the **`lan`** command:

```
R>lan
lan is enabled
   Link Status is UP
   100BaseTX
  lan -i 15.5.24.116
  lan -g 15.5.23.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address : 08000909BAC1
R>
```

The Ethernet address, also known as the link level address, is preassigned at the factory, and is printed on a label on the FPGA trace port analyzer.

8 Change the LAN parameters by entering **`lan`** commands using the following syntax:

```
lan -i <internet> [-g <gateway>] [-p <port>] [-s
<subnet>]
```

The lan command parameters are:

`-i <internet>` The IP address which you obtained from your network administrator.

`-g <gateway>` The gateway address. Setting the gateway address allows access outside your local network or subnet.

`-s <subnet>` This changes the subnet mask.

`-p <port>` This changes the base TCP service port number, normally 6470.

Do not change the default port numbers (6470, 6471) unless they conflict with some other product on your network. The numbers must be greater than 1024. If you change the base port, enter the new value in the configuration of your Xilinx ChipScope software (and, for UNIX workstations, in the /etc/services file).

Example

To assign an IP address of 192.6.94.2 to the FPGA trace port analyzer, enter the following command:

```
R>lan -i 192.6.94.2
```

If there are serial port connection problems

If the FPGA trace port analyzer prompt does not appear in the terminal emulator window (or terminal display) after pressing the Return or Enter key:

❏ Make sure that you have connected the FPGA trace port analyzer to the proper power source and that the power switch is on.

With certain serial (RS-232) port interface cards, connecting to a serial port when the FPGA trace port analyzer is turned off (or is not connected) will hang the personal computer. The only way to get control back is to reboot the computer. Therefore, we recommend that you always turn on the FPGA trace port analyzer before attempting to connect via a serial port.

❏ Make sure the serial cable is connected to the correct serial port on your computer (or terminal).

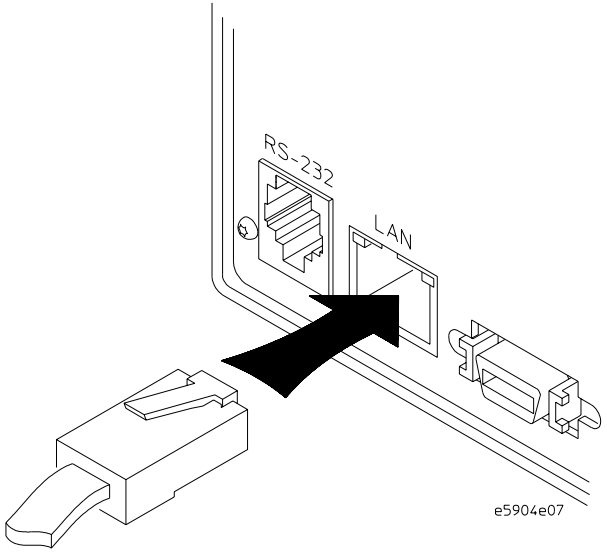
❏ Make sure you are using the serial cable and adapter which are supplied with the FPGA trace port analyzer.

❏ Make sure that you have properly configured the terminal emulator (or terminal) data communications settings:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

Step 3. Connect the LAN cable

- Connect the LAN cable to the connector on the FPGA trace port analyzer.



Be sure to use the appropriate Category 3 or Category 5 cable for your LAN.

Step 4. Cycle power on the FPGA trace port analyzer

1. Cycle power on the FPGA trace port analyzer by powering it off then on again.

   When using DHCP, you must cycle power in order for the FPGA trace port analyzer to send out a DHCPDISCOVER packet so that its LAN parameter settings can be set automatically by a server.

   When using a serial connection, you must cycle power in order for the FPGA trace port analyzer's LAN parameter changes to take effect.

2. Wait at least 20 seconds for the FPGA trace port analyzer to recognize the LAN.

3. Once the FPGA trace port analyzer has been connected to the LAN, it can communicate with computers on the network.

Step 5. Run Xilinx ChipScope Pro software

The Agilent Technologies E5904B Option 500 FPGA trace port analyzer is used with Xilinx ChipScope Pro software. Refer to Xilinx ChipScope Pro documentation for information on opening a connection with the Agilent FPGA trace port analyzer.

4

Configuring the Trace Port Analyzer

After you have established communications with the FPGA trace port analyzer from the Xilinx ChipScope Pro software, you may need to set certain configuration items appropriately for your target system (such as JTAG communication speed). Use the Xilinx ChipScope Pro software to change the configuration items.

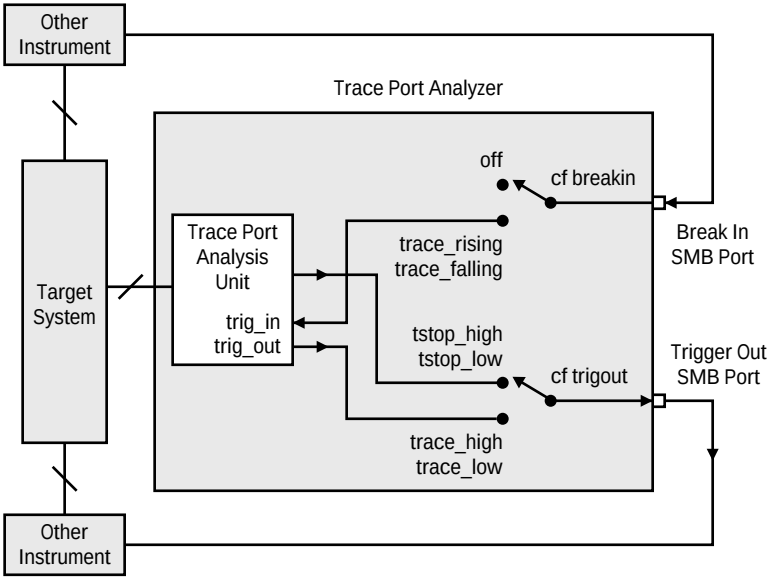
The Xilinx ChipScope Pro software lets you save FPGA trace port analyzer configuration settings to a file so they can be used to re-configure the FPGA trace port analyzer at the beginning of each Xilinx ChipScope Pro software session. Refer to the ChipScope Pro documentation for instructions.

To configure the Trigger Out SMB port

Value	The Trigger Out SMB will...	Built-in command
fixhigh	always be high.	cf trigout=fixhigh
fixlow	always be low.	cf trigout=fixlow
tstop_high	go high when the trace is has stopped.	cf trigout=tstop_high
tstop_low	go low when the trace is has stopped.	cf trigout=tstop_low
trace_high	go high when the trace port trigger occurs. (Default)	cf trigout=trace_high
trace_low	go low when the trace port trigger occurs.	cf trigout=trace_low

To configure the Break In SMB port

Value	Break In SMB	Built-in command
off	Inputs to the Break In SMB will be ignored.	cf breakin=off
trace_rising	A rising edge on the break in SMB port will cause the FPGA trace port analyzer to trigger.	cf breakin=trace_rising
trace_falling	A falling edge on the break in SMB port will cause the FPGA trace port analyzer to trigger.	cf breakin=trace_falling



5

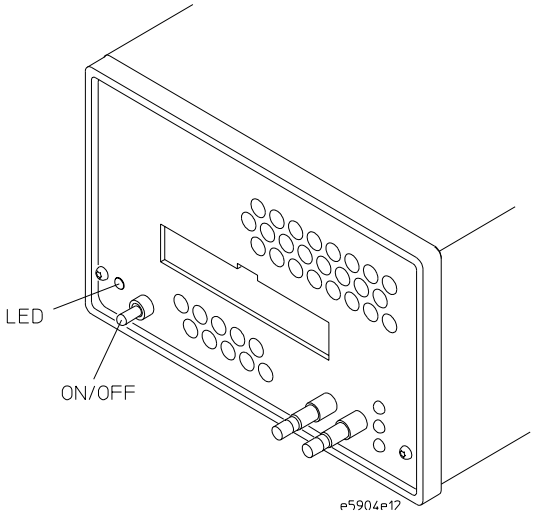
Connecting to a Target System

After the FPGA trace port analyzer has been properly configured for the target system, you can connect it to the target system and verify its operation.

Connecting the FPGA Trace Port Analyzer to the Target System

Step 1. Turn OFF power to the target system.

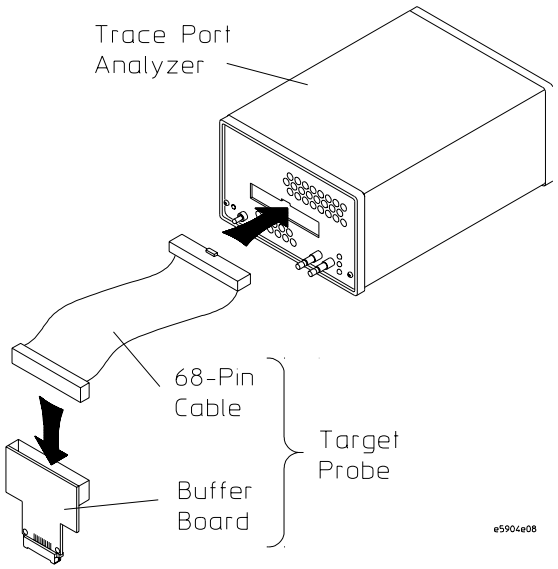
Step 2: Turn OFF the FPGA trace port analyzer power switch.



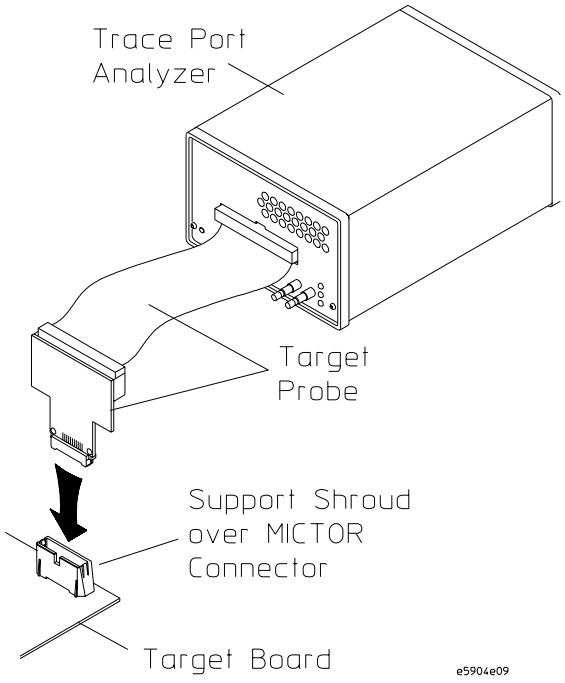
Step 3. Connect the FPGA trace port analyzer to the target probe

1 Plug one end of the 68-pin cable into the FPGA trace port analyzer.

2 Plug the other end of the 68-pin cable into the connector on the buffer board.



Step 4. Plug the target probe into the target system MICTOR header connector.



Step 5. Turn ON the FPGA trace port analyzer power switch.

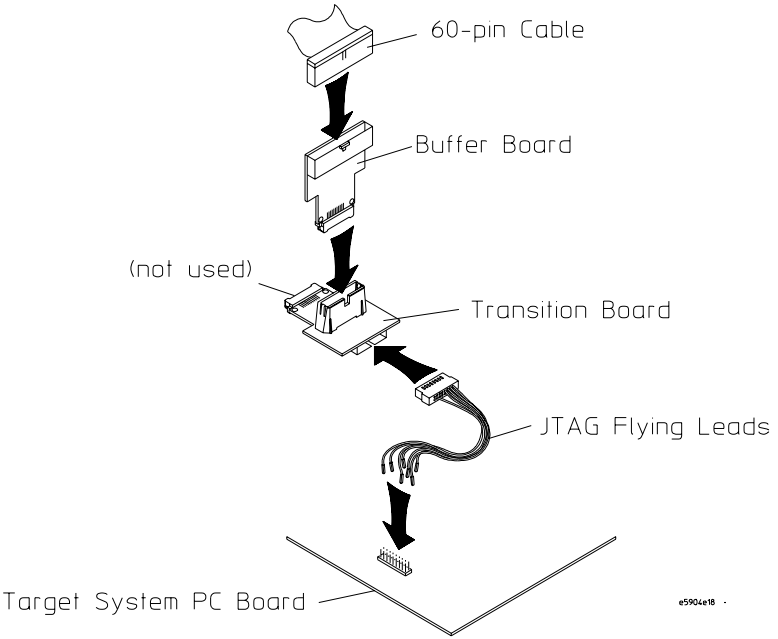
Step 6. Turn ON power to the target system.

Using a Non-Standard Header Connector

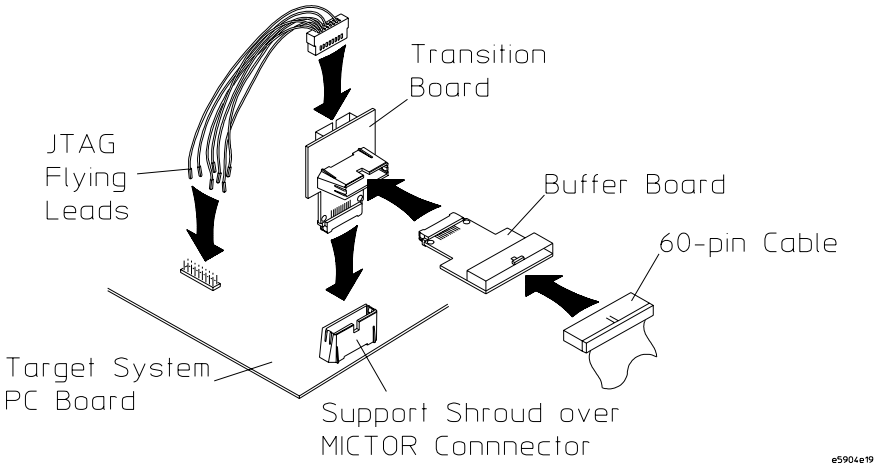
For target systems that do not comply with the connector pinout shown on page 29, a transition board and JTAG flying lead set are provided.

The transition board supports the following two scenarios:

- The target system PC board does not have a MICTOR connector for trace; it only has a JTAG header.



- The target system has a MICTOR for trace, but the JTAG lines were not connected to the MICTOR.



See Also

See the non-standard connector pinout information on page 37.

See "JTAG Flying Lead Set Pinout" on page 39.

Verifying the Target System Connection

After the FPGA trace port analyzer has been plugged into the target system, you should verify that the FPGA trace port analyzer works correctly.

To verify FPGA trace port analyzer operation

❏ Perform some simple tests in the Xilinx ChipScope Pro software to verify that the FPGA trace port analyzer is working properly with the target system.

If the FPGA trace port analyzer doesn't work with the Xilinx ChipScope Pro software

Most problems are associated with not having the FPGA trace port analyzer and target system properly configured or initialized.

❏ Initialize the FPGA trace port analyzer and target system so that the Xilinx ChipScope Pro software can connect.

Refer to your Xilinx ChipScope Pro software manual for proper initialization.

If there are target system interaction problems

❏ See "Verifying JTAG Interaction with the Target System" on page 95.

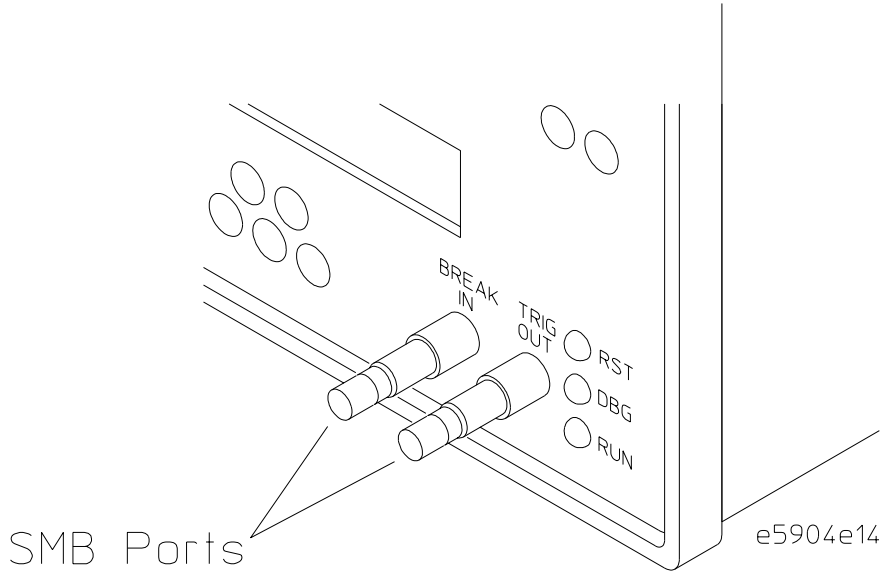
6

Coordinating Measurements with Other Test Instruments

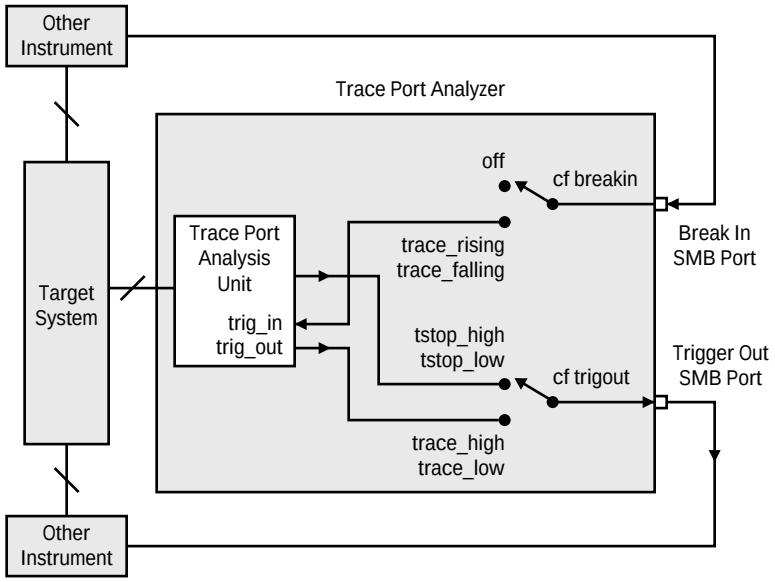
You can make coordinated measurements when you want to correlate real-time trace data from the ILA with data captured by other test instruments (for example, a logic analyzer that captures data from other parts of your target system).

The Agilent Technologies E5904B Option 500 FPGA trace port analyzer has two SMB ports for coordinating measurements with other test instruments:

- Trigger Out SMB port.
- Break In SMB port.



By using the FPGA trace port analyzer's "trigout" and "breakin" configuration options, you can route the Trigger Out and Break In signals to either the JTAG unit or to the trace port analysis unit.



Receiving a Break In Signal from Another Test Instrument

You can use the FPGA trace port analyzer's Break In signal to allow another test instrument to trigger the trace port analysis unit.

To specify when to trigger the FPGA trace port analyzer

When another test instrument detects a problem, you might want to see what the FPGA is doing when the problem occurs.

1. Connect the other test instrument's output to the FPGA trace port analyzer's Break In SMB port.
2. Set the FPGA trace port analyzer's "breakin" configuration item to either "trace_rising" or "trace_falling" (depending on whether the other test instrument outputs a rising edge or a falling edge).
3. Start the FPGA trace port analysis unit's measurement.
4. Start the other test instrument's measurement.

See Also

"To configure the Break In SMB port" on page 61.

Driving a Trigger Out Signal to Another Test Instrument

You can use the FPGA trace port analyzer's Trigger Out signal to:

- Indicate to another test instrument when trace is complete or stops.
- Indicate to another test instrument when the trace port analysis unit's trigger occurs.

To indicate when trace is complete or stops

You might want to do this, for example, to qualify a (synchronous) state logic analyzer's sampling clock so that it captures data only when the FPGA is storing trace.

1. Connect the FPGA trace port analyzer's Trigger Out SMB port to the other test instrument's input.
2. Set the FPGA trace port analyzer's "trigout" configuration item to either "tstop_high" or "tstop_low" (depending on whether the other test instrument expects an active high or an active low signal).
3. Start the other test instrument's measurement.
4. Run the trace port analysis unit's measurement.

See Also "To configure the Trigger Out SMB port" on page 60.

To indicate when the trace port trigger occurs

You may want to use the trace port analysis unit, for example, to trigger other test instruments like oscilloscopes or logic analyzers which are looking at other parts of the target system.

1. Connect the FPGA trace port analyzer's Trigger Out SMB port to the other test instrument's input.
2. Set the FPGA trace port analyzer's "trigout" configuration item to either "trace_high" or "trace_low" (depending on whether the other test instrument expects a rising edge or falling edge to signal when the trigger occurs).
3. Start the other test instrument's measurement.
4. Run the trace port analysis unit's measurement.

See Also "To configure the Trigger Out SMB port" on page 60.

7

Updating Firmware

If there is a newer version of firmware for the Agilent Technologies E5904B Option 500 FPGA trace port analyzer, you can update it using the procedures described in this chapter.

To display current firmware version information

1. Use the "telnet" command from a networked computer to access the FPGA trace port analyzer's built-in command interface.
2. Enter the built-in "ver -a" command to view the version information for firmware currently in the FPGA trace port analyzer.

Example

```
J>ver

         Copyright (c) Agilent Technologies, Inc. 1999
All Rights Reserved.  Reproduction, adaptation, or translation without prior
written permission is prohibited, except as allowed under copyright laws.

  HPE8130A Series Emulation System
    Version:   A.01.21 27Jun02
    Location:  Generics

  HPE3486A FPGA Trace Port Analyzer
    Version:   A.05.12 08Jul02
J>
```

To get firmware from the web

To update the firmware, you must have access to the World Wide Web and a personal computer or a workstation connected to your FPGA trace port analyzer.

1. Download the new firmware from the following World Wide Web site:

   http://www.cos.agilent.com/probe/

2. Follow the instructions on the web site for installing the firmware.

To update firmware from a floppy disk

- Follow the instructions on the README file on the floppy disk.

  The firmware can be installed using either a personal computer or a workstation which can read personal computer floppy disks.

8

Solving Problems

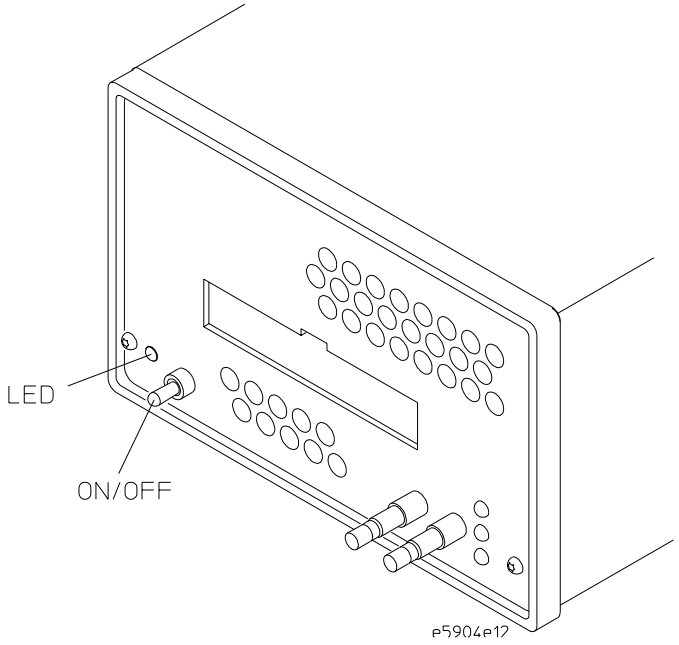
Problems with the FPGA trace port analyzer can occur in:

- The connection between the FPGA trace port analyzer and the Xilinx ChipScope Pro software.
- The FPGA trace port analyzer itself.
- The connection between the FPGA trace port analyzer and the target system.
- The target system.

You can use the procedures in this chapter to identify the source of problems.

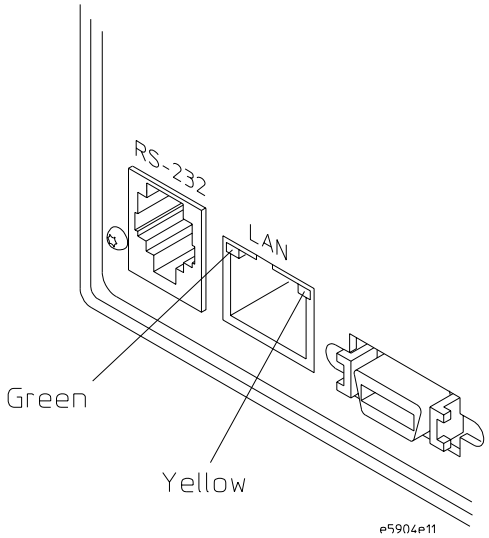
Interpreting the Trace Port Analyzer Status Lights

Power ON Light



The green LED, to the left of the power switch, is lit when the FPGA trace port analyzer is connected to a power source and the power switch is on.

LAN Status Lights



The yellow LED, on the right side of the connector, indicates LAN activity (receive or transmit).

The green LED, on the left side of the connector, is lit when the LAN interface is operating in 100Base-TX mode.

Verifying FPGA Trace Port Analyzer LAN Communications

Follow these steps if there are problems establishing LAN communications to the FPGA trace port analyzer from the Xilinx ChipScope Pro software or by using telnet on a networked computer.

Step 1. Verify the physical connection

1 Make sure that the proper LAN cable is connected.

- Use a Category 5 cable if your connection is running at 100 Mbps (100BASE-TX).
- Use a Category 3 cable if your connection is running at 10 Mbps (10BASE-T).

2 With the FPGA trace port analyzer powered on, look at the LAN status lights to verify that the FPGA trace port analyzer is seeing LAN activity.

See “LAN Status Lights” on page 84. No activity indicates a problem with the LAN port or cable. Contact your network system administrator.

Step 2. Use the “ping” command on a networked computer

These instructions assume you are using a personal computer running Microsoft® Windows®. The procedure for other operating systems is slightly different.

1 Open an MS-DOS Command Prompt window, or choose Start->Run....

2 Enter the "ping" command followed by the IP address of the FPGA trace port analyzer.

Example

```
C:\WINDOWS>ping 15.6.253.138

Pinging 15.6.253.138 with 32 bytes of data:

Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time<10ms TTL=254
```

3 If ping gets replies from the FPGA trace port analyzer (but you are unable to telnet to it), try rebooting the FPGA trace port analyzer by turning its power switch off then on again.

Problems with FPGA trace port analyzer firmware could lead to situations where the LAN interface is up and running but you are not able to telnet to the FPGA trace port analyzer or, if you are able to telnet to the FPGA trace port analyzer, you are not able to enter commands.

If there are LAN connection problems

If the results of the "ping" command shows something like "100% packet loss" or "Destination host unreachable":

- ❑ Make sure that you have connected the FPGA trace port analyzer to the proper power source and that the power light is lit.
- ❑ Make sure that you wait for the power-on self test to complete before connecting.
- ❑ If you have just changed the IP address of the FPGA trace port analyzer, leave the FPGA trace port analyzer powered on and connected to the LAN for a few minutes, then try again.

  Some hubs, routers, and hosts maintain tables of IP addresses and link-level addresses. It may take a while for these tables to be updated.

- ❏ Make sure that the FPGA trace port analyzer's IP address is set up correctly.

  To do this, repeat the steps shown in "To set LAN parameters using a serial port connection" on page 50.

- ❏ If the FPGA trace port analyzer is on a different subnet than the host computer, make sure that the gateway address is set up correctly.

  The default gateway address of 0.0.0.0 does not allow the FPGA trace port analyzer to communicate with computers on other subnets.

If it takes a long time to connect to the network

- ❏ Check the subnet masks on the other LAN devices connected to your network. All of the devices should be configured to use the same subnet mask.

  Subnet mask error messages do not indicate a major problem. You can continue using the FPGA trace port analyzer.

  If there are many subnet masks in use on the local subnet, the FPGA trace port analyzer may take a very long time to connect to the network after it is turned on.

If ChipScope Pro cannot communicate with the FPGA trace port analyzer

- ❏ Check that ChipScope Pro is using the correct IP address for the FPGA trace port analyzer.

  Refer to the Xilinx ChipScope Pro manual for information on specifying the FPGA trace port analyzer's IP address.

- ❏ Telnet to the FPGA trace port analyzer from the same networked computer that runs the Xilinx ChipScope Pro software (see "To

'telnet' to the FPGA trace port analyzer").

If Xilinx ChipScope Pro uses the network *hostname* for the FPGA trace port analyzer (which doesn't work) and the telnet command uses the network *IP address* (which does work), the problem could be with the name server or host table lookup mechanism. If this is the case, try using the FPGA trace port analyzer's IP address in the Xilinx ChipScope Pro software.

If the telnet connection doesn't work, refer to "Verifying Trace Port Analyzer LAN Communications" in the "Solving Problems" chapter.

To "telnet" to the FPGA trace port analyzer

1 Verify your FPGA trace port analyzer is now active and on the network by issuing a telnet command from a networked computer to the FPGA trace port analyzer's IP address.

Example

```
$ telnet 192.35.12.6
J>
J>
```

If you do not see a prompt, press the Return or Enter key a few times.

This connection will give you access to the FPGA trace port analyzer's built-in command interface.

2 To enter a command, type it in at the built-in command interface prompt, and press the Return or Enter key.

For example, to view the LAN parameters, enter the "lan" command.

Example

```
J>lan
lan is enabled
   Link Status is UP
   10BaseT
  lan -i 130.29.66.134
  lan -g 130.29.64.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address: 0030D300A10C
```

3 To exit from the telnet session, type Ctrl+D at the prompt.

Using the Trace Port Analyzer's Built-In Commands

The FPGA trace port analyzer has a built-in command interface which you can use for configuring or troubleshooting the FPGA trace port analyzer.

You can access the built-in command interface via:

- A telnet (LAN) connection.
- A serial connection (as may have been used in "To set LAN parameters using a serial port connection" on page 50).

Command Prompts

The prompt indicates the status of the FPGA trace port analyzer:

J	JTAG status: ready
Z	Buffer board not connected or recognized
?	Unknown state

Commonly Used Commands

Command	Description
cf	Configuration—read or write configuration options.
help	Help—display online help for built-in commands
init	Initialize—**init -c** re-initializes everything in the trace port analyzer except for the LAN software.
lan	Configure LAN parameters.
tlist	Display data captured by the trace port analysis unit.
trun	Start the trace port analysis unit's measurement.
tstatus	Display whether the trace port analysis unit is "running" or "stopped".
tstop	Stop the trace port analysis unit's measurement.
ver	Version—display the product number and firmware version of the trace port analyzer.

Use **? <command>** (or **help <command>**) to show the command syntax and required parameters for each command. For example, enter **? tstop** to show syntax and required parameters for the trace stop command.

Examples

```
J>? tstop
tstop [-a|-m] - stop the trace port analyzer from run-
ning
```

Note that some commands listed in the help screens are generic commands and may not be available for your FPGA trace port analyzer.

Checking the Initial Trace Port Analyzer Status

After establishing a telnet connection to the FPGA trace port analyzer, an initial status prompt of “->” or “?>” indicates a problem.

If the prompt is “->”

The "->" prompt indicates that the FPGA trace port analyzer is not connected to a target probe (which is the 68-pin cable and a buffer board) or that the firmware loaded into the FPGA trace port analyzer is not compatible with its hardware.

Try one of the following until you get a different prompt:

- ❏ If the FPGA trace port analyzer is not connected to the target probe, connect the target probe and enter the “init -c” command to re-initialize.
- ❏ Cycle power on the FPGA trace port analyzer. (Turn off target system power first.)
- ❏ Check that the proper firmware is installed by entering the “ver” command.

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 7, “Updating Firmware,” on page 77.
- ❏ Run the FPGA trace port analyzer performance verification tests to make sure it is working correctly.

  Refer to “Running Trace Port Analyzer Performance Verification Tests” on page 97.

If the prompt is “?>”

The "?>" prompt indicates that the FPGA trace port analyzer is having trouble communicating with the target system. The FPGA trace port analyzer doesn’t know what state the target system is in.

❑ Follow the procedure in the “Verifying JTAG Interaction with the Target System” on page 95.

Verifying JTAG Interaction with the Target System

Use the ChipScope Pro software to determine whether the JTAG port is operating properly with the target system. See the ChipScope Pro software documentation for information on initializing the JTAG scan chains.

If the FPGA trace port analyzer has problems controlling the target system

The FPGA trace port analyzer might be having problems controlling the target if you are unable to initialize the JTAG scan chain with the ChipScope Pro software.

Problems controlling the target can be caused by a variety of conditions. Typically the problem is in the configuration of the FPGA trace port analyzer or the configuration of the target system.

Try the following to better control your target system:

- ❏ Check that the FPGA trace port analyzer is connected to the target system. See page 65.
- ❏ Decrease the JTAG communication speed. Some target systems need slower speeds to properly communicate.

  Use the ChipScope Pro software to reduce the JTAG communication speed.
- ❏ Check that the target FPGA programmed.

  Use the ChipScope Pro software to program your FPGA.
- ❏ Check that the proper firmware is installed in the FPGA trace port analyzer by entering the “ver” command (see “To display current firmware version information” on page 78).

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 7, “Updating Firmware,” on page 77.

Running Trace Port Analyzer Performance Verification Tests

In addition to the powerup tests, there are several additional performance verification (PV) tests available.

These tests can be performed using either a LAN connection or a serial port (RS-232) connection.

Step 1. Prepare for the performance verification tests

You will need the Agilent E5903-66509 PV board and an SMB cable (such as Agilent 16532-61601) to perform the performance verification tests. The PV board is supplied with the Agilent E5904 Option 500 FPGA trace port analyzer; the SMB cable is not.

1. End any ChipScope Pro sessions.
2. Power OFF the target system.
3. Power OFF the FPGA trace port analyzer.
4. Disconnect the FPGA trace port analyzer from the target system.

CAUTION: If the FPGA trace port analyzer is not disconnected from the target system and the performance verification tests are run, the Target Board Adapter Feedback Test can damage components on the target system.

5. Connect the E5903-66509 PV board to the 68-pin cable of the FPGA trace port analyzer.
6. Connect an SMB (f) to SMB (f) cable (such as Agilent 16532-61601) from the "Break In" connector to the "Trigger Out" connector on the FPGA trace port analyzer.

   If you aren't concerned about these signals, you may omit this step and

ignore any related test failures.

7 Turn the FPGA trace port analyzer on again.

8 Access the FPGA trace port analyzer's built-in command interface.

If you're using a LAN connection, you can **`telnet`** to the FPGA trace port analyzer from a computer on the network and enter commands (see "To "telnet" to the FPGA trace port analyzer" on page 88).

If you're using a serial port (RS-232) connection, you can connect a terminal emulator or an actual terminal to the FPGA trace port analyzer and use it to enter commands (see "To set LAN parameters using a serial port connection" on page 50).

Step 2. Enter the "pv" command

Options available for the **`pv`** command are explained in the help screen displayed by typing **`help pv`** or **`? pv`** at the prompt.

1 Enter the **`pv 1`** command.

The results on a good system, with the trigger out and break in SMBs connected, should look similar to the following.

```
J>pv 1

  Testing: HPE8130A Series Emulation System
    Test  1: Powerup PV Results                          Passed!
    Test  2: Emulation Module Port Feedback Test         Passed!
    Test  3: Run Control FPGA Test                       Passed!
    Test  4: Run Control Clock Test                      Passed!
    Test  5: Break In and Trigger Out SMB Feedback Test  Passed!
  Testing: HPE3486A FPGA Trace Port Analyzer
    Test  1: Trace Board Feedback Test                   Passed!
    Test  2: Target Probe Feedback Test                  Passed!
  PASSED  Number of tests: 1          Number of failures: 0

Target Probe ID 0x7, Cpld ID 0x3
Aztec Programmed and ready

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  HPE8130A Series Emulation System
    Version:   A.01.21 27Jun02
    Location:  Generics

  HPE3486A FPGA Trace Port Analyzer
    Version:   A.05.12 08Jul02
J>
```

2 If a performance verification test fails, enter the **`pv -v3 1`** command.

Details of the failure can be seen by entering the "pv" command again with a verbose level of 3.

If the powerup PV results test fails

Failure of the Powerup PV Results test indicates a hardware problem with the FPGA trace port analyzer.

❑ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

If the emulation module port feedback test fails

Failure of the Emulation Module Port Feedback Test indicates a hardware problem with the FPGA trace port analyzer.

❑ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

This test exercises the hardware which drives the connection to the FPGA trace port analyzer.

If the JTAG FPGA test fails

Failure of the Run Control FPGA Test indicates a hardware problem with the FPGA trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

If the FPGA trace port analyzer fails this test, it may have been damaged by electrostatic discharge through the target cable. To prevent such damage in the future, follow standard ESD preventive practices.

If the JTAG clock test fails

Failure of the Run Control Clock Test indicates a hardware problem with the FPGA trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

If the FPGA trace port analyzer fails this test, it may have been damaged by electrostatic discharge through the target cable. To prevent such damage in the future, follow standard ESD preventive practices.

If the break in and trigger out SMB feedback test fails

If the Break In and Trigger Out SMB Feedback Test fails:

❏ Make sure you have connected a good cable between the two SMB connectors.

❏ If the cable is good, contact Agilent Technologies for assistance

(see "Contacting Agilent Technologies" on page 102).

If the trace board feedback test fails

Failure of the Trace Board Adapter Feedback Test indicates a hardware problem with the FPGA trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

If the target probe feedback test fails

Failure of the Target Probe Feedback Test indicates a hardware problem with the FPGA trace port analyzer.

❏ Make sure the target probe (that is, the 68-pin cable and the appropriate buffer board) is connected to the FPGA trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 102).

Contacting Agilent Technologies

If the FPGA trace port analyzer still does not work after following the troubleshooting steps in this chapter:

1. Write down the target FPGA version, the FPGA trace port analyzer firmware version, and the FPGA trace port analyzer model number (Agilent Technologies E5904B Option 500).
2. Call your nearest Agilent Technologies sales or service office.

   To locate a sales or service office near you, go to the world-wide web site:

   http://www.tm.agilent.com

   and select Contact Us.

9

Characteristics

This chapter describes the following characteristics of the Agilent Technologies E5904B Option 500 FPGA trace port analyzer:

- Input/output electrical characteristics.
- JTAG controller characteristics.
- Trace port analysis characteristics.
- Environmental characteristics.

Input/Output Electrical Characteristics

Trigger Out SMB Port

With a 50 Ω load, a logic high is ≥ 2.0 V, and a low is ≤ 0.4 V. The output function is selectable (see "To configure the Trigger Out SMB port" on page 60).

Break In SMB Port

Edge-triggered TTL level input, 20 pF, with 4.6 kΩ to ground in parallel. Maximum input: +5 V to -5 V when the FPGA trace port analyzer is powered OFF; +10 V to -5 V when the FPGA trace port analyzer is powered ON. Input function is selectable (see "To configure the Break In SMB port" on page 61).

Communication Ports

Serial Port

RJ12 connector (DB9-to-RJ12 adapter and serial cable included). RS-232 DCE to 115.2 kbaud.

IEEE 802.3 Type 10/100Base-TX LAN Port

RJ-45 connector, is compatible with both 10 Mbps (10Base-T) and 100 Mbps (100Base-TX) twisted-pair ethernet LANs.

Power Supply

Input. 100-240 V, 1.0 A, 50/60 Hz, IEC 320 connector.

Output. 12 V, 3.3 A

CAT I (Mains isolated).

JTAG controller Characteristics

FPGA Compatibility

The Agilent Technologies E5904B Option 500 FPGA trace port analyzer supports the Xilinx FPGA families listed on page 6.

Electrical Characteristics

TDO Input Characteristics							
Signal	**Symbol**	**1/3 Vref**		**1/2 Vref**		**2/3 Vref**	
		Min	**Max**	**Min**	**Max**	**Min**	**Max**
TDO	Vih	0.5 Vref	5.1 V	0.65 Vref	5.1 V	0.8 Vref	5.1 V
	Vil	-0.1V	0.2 Vref	-0.1 V	0.35 V	-0.1 V	0.5 Vref
	Ib (Bias)	± 15 uA					
	Rin	4.7 kΩ pullup to Vref					
	Cin	TDO = 75 pF, DBGACK = 95 pF, RTCK = 80 pF					

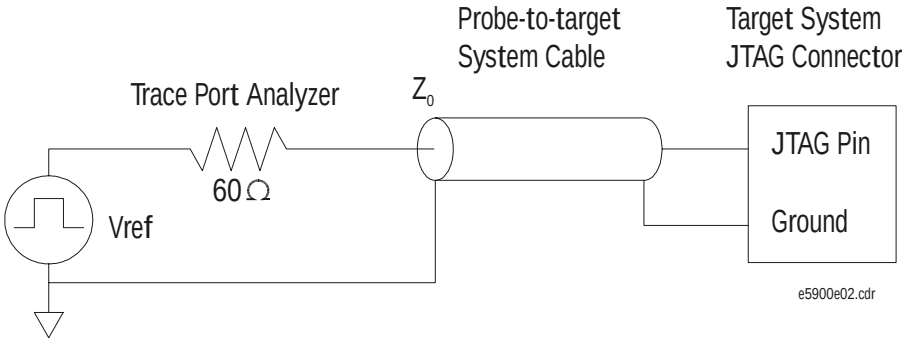
Vref Input Characteristics			
Signal	**Symbol**	**Min**	**Max**
Vref[1]	Vin	1.65 V	3.6 V
	Rin	25 kΩ pulldown to ground	

[1] Vref is used to determine the target power status and the reference for input threshold and output voltage swings. The trace port analyzer does not draw power from this source.

Output Signal Characteristics		
Signal	**Symbol**	**Condition**
TDI, TCK, TMS	Voh/Ioh	66 Ω ± 15 Ω to Vref
	Vol/Iol	66 Ω ± 15 Ω to 0.2 V

Output Model

This is the model of output drive to TDI, TCK, and TMS.



Note: Z_o = 66 Ω in the diagram above.

Trace Port Analysis Unit Characteristics

For the characteristics of the trace port analysis unit, see:

- "Signal Requirements" on page 31.
- "Buffer Board—Required Voltage Levels" on page 32.
- "Loading Effects" on page 33.

Environmental Characteristics

Temperature	Operating: +5 degrees to +40 degrees C (+41 to +104 degrees F) Non-operating: -40 degrees to +70 degrees C (-40 to +158 degrees F).
Relative Humidity	15% to 95%
Pollution Degree	Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.
Altitude	Operating or non-operating: 4600 m (15 000 ft.).
For indoor use only.	

10

Service Guide

To get replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. The part numbers are subject to change. Contact your nearest Agilent Technologies sales office for further information (see "Contacting Agilent Technologies" on page 102).

Replacement assemblies

Part number	Description
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Power supply ferrite kit
E5903-61602	68-pin cable
E5903-66507	Buffer board
E3486-66503	Transition board (only required for non-standard header)
E5903-66509	PV board
E8130-68702	Serial cable and adapter

NOTE: See the figure on page 7 for an illustration of most of these replacement parts.

To exchange a faulty assembly for a repaired and tested assembly

The following item has been set up on the Agilent Technologies exchange assembly program. You can exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchange assemblies

Part number	Description
E5840-69501	Rebuilt FPGA trace port analyzer (accessories not included)

To return a part to Agilent Technologies for service

1. Follow the procedures in the "Solving Problems" chapter to make sure that the problem is caused by a hardware failure and not by configuration or cabling problems.
2. Get the address of the nearest Agilent Technologies service center.

   See "Contacting Agilent Technologies" on page 102.
3. Package the part and send it to the Agilent Technologies service center.

   Keep any parts which you know are working. For example, if only a cable is broken, keep the FPGA trace port analyzer.
4. When the part has been replaced, it will be sent back to you.

   The unit returned to you will have the same serial number as the unit you sent to Agilent Technologies.

   In some parts of the world, on-site repair service is available. Ask an Agilent Technologies sales or service representative for details.

To clean the instrument

If the instrument requires cleaning:

1. Remove power from the instrument.
2. Clean the instrument using a soft cloth that has been moistened in a mixture of mild detergent and water.
3. Make sure that the instrument is completely dry before reconnecting it to a power source.

D

debug port A hardware interface designed into a microprocessor that allows developers to control microprocessor execution, set breakpoints, and access microprocessor registers or target system memory using a tool like the emulation probe.

device under test Another name for a target system under development.

H

hostname A name that is associated with the IP address of a device on the network.

I

IP address An address, in integer dot notation (for example, 15.6.240.253), that is given to a device on the network.

J

JTAG port See *debug port*.

JTAG interface unit See *run control unit*.

L

LAN name See *hostname*.

T

target system The device under test that is being developed and debugged.

threshold voltage The level at which voltages above are logic "highs" (1) and voltages below are logic "lows" (0).

trace port analyzer A tool that collects trace information and presents it to ChipScope Pro.

trigger specification A set of conditions that must be true before the instrument triggers.

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DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Manufacturer's Name:	Agilent Technologies
Manufacturer's Address:	1900 Garden of the Gods Road Colorado Springs, CO 80907 USA

Declares, that the product

Product Name:	Trace Port Analyzer
Model Number(s):	E5904B
Product Option(s):	This declaration covers all options of the above product(s).

Conforms to the following product standards:

	Standard	Limit
EMC	IEC 61326:2002 / EN 61326:1997+A1:1998+A2:2001	
	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-4:1995	4 kV CD, 8 kV AD
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	3 V/m, 80-1000 MHz
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	0.5 kV Sig. Lines, 1 kV Power Lines
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	3V, 0.15-80 MHz
Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995	
	Canada: CSA-C22.2 No. 1010.1:1992	

Conformity/Supplemental Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE marking accordingly (European Union).

This product was tested in a typical configuration with Agilent Technologies test systems.

Date: 7/10/2002

Ken Wyatt, Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.

Ken Wyatt

Product Regulations

EMC	Standard	Performance Criteria
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991—Group 1 Class A	
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-4:1995 (ESD 4 kV CD, 8 kV AD)	A (See Note)
	IEC 61000-4-3:1995 / EN 61000-4-3:1995 (3 V/m 80% AM)	A
	IEC 61000-4-4:1995 / EN 61000-4-4:1995 (EFT 0.5 kV line-line, 1 kV line-earth	A
	IEC 61000-4-6:1996 / EN 61000-4-6:1996 (3V, 80% AM, power line)	A
	Regulatory Information for Canada	
	ICES/NMB-001:1998	
	This ISM device complies with Canadian ICES-001.	
	Cet appareil ISM est confomre à la norme NMB-001 du Canada.	
	Regulatory Information for Australia/New Zealand	
	This ISM device complies with Australian/New Zealand AS/NZS 2064.1 N10149	
Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995	
	Canada: CSA-C22.2 No. 1010.1:1992	

Additional Information

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE marking accordingly (European Union).

Performance Criteria:
A PASS - Normal operation, no effect.
B PASS - Temporary degradation, self recoverable.
C PASS - Temporary degradation, operator intervention required.
D FAIL - Not recoverable, component damage.

Note: The target probe (cable plus buffer board) is ESD sensitive. Use standard ESD preventive practices to avoid component damage.

Sound Pressure Level Not Applicable

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

• If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product..

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Agilent Technologies Inc.
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Notices

Manual Part Number

E3486-97001, December 2002

Print History

E3486-97001, December 2002
E3486-97000, August 2002

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1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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